SVRPlus-CSI2-I
Extended
MIPI CSI2
High Performance
Serial Video Receiver
IP Core Family

Information Brief

Introduction

This document is a short description of VLSI Plus (www.vlsiplus.com) SVRPlus-CSI2-1 – a family of second generation high performance Serial Video Receivers for video streams, supporting MIPI CSI2 and extensions to MIPI CSI2, and allowing very high performance while employing relatively low clock frequencies.

The SVRPlus-CSI2-1 definition and design take advantage from the long experience of VLSI Plus in providing first generation CSI2 receiver IP cores to a variety of customers. VLSI Plus SVR-CS and SVR-CS4 are used by leading CMOS image sensor vendors for the production floor testing of their sensor modules. Continued dialog with CSI2 customers in the past five years enabled us to define this new generation CSI2 receiver IP to meet current and future needs.

The family is aimed at ASIC implementation, and includes the following products:

a. SVRPlus-CSI2-I-41: 4 data lanes, one pixel output per clock
b. SVRPlus-CSI2-I-42: 4 data lanes, two pixel output per clock
c. SVRPlus-CSI2-I-44: 8 data lanes, four pixel output per clock
d. SVRPlus-CSI2-I-81: 8 data lanes, one pixel output per clock
e. SVRPlus-CSI2-I-82: 8 data lanes, two pixel output per clock
f. SVRPlus-CSI2-I-84: 8 data lanes, four pixel output per clock

For reader convenience, we will refer to groups of the IP cores above as follows:

- Products a, b and c: SVRPlus-CSI2-I-4X
- Products d, e and f: SVRPlus-CSI2-I-8X
- Products a and d: SVRPlus-CSI2-I-X1
- Products b and e: SVRPlus-CSI2-I-X2
- Products c and f: SVRPlus-CSI2-I-X4

Need for Higher Data Rates

Latest and forthcoming CMOS image sensors surpass 10M pixels, and output video at 30 and even 60 fps. This development requires high bandwidth between the camera and the application processor. For example, a commercially available 4068x3456 30 fps camera outputs an average of over 5Gbps, which requires 4 DPHY lanes at more than 1.25Gbp – more the original 1Gpbs of MIPI® DPHY 1.0, but still manageable by the extended 1.5Gbps of the latest DPHY spec. However, when the same or similar camera will reach 60fps, over 10Gbps will be required, and 4 lanes will not suffice.

MIPI®'s forthcoming new set of standards (CSI3 over UNIPRO and MPHY) will offer higher bandwidth. However, until those standards are available, camera vendors are

looking for ways to increase CSI2 speed. Among others, extension of the CSI2 standard to 8 data lanes, with one or two clock lanes, are introduced.

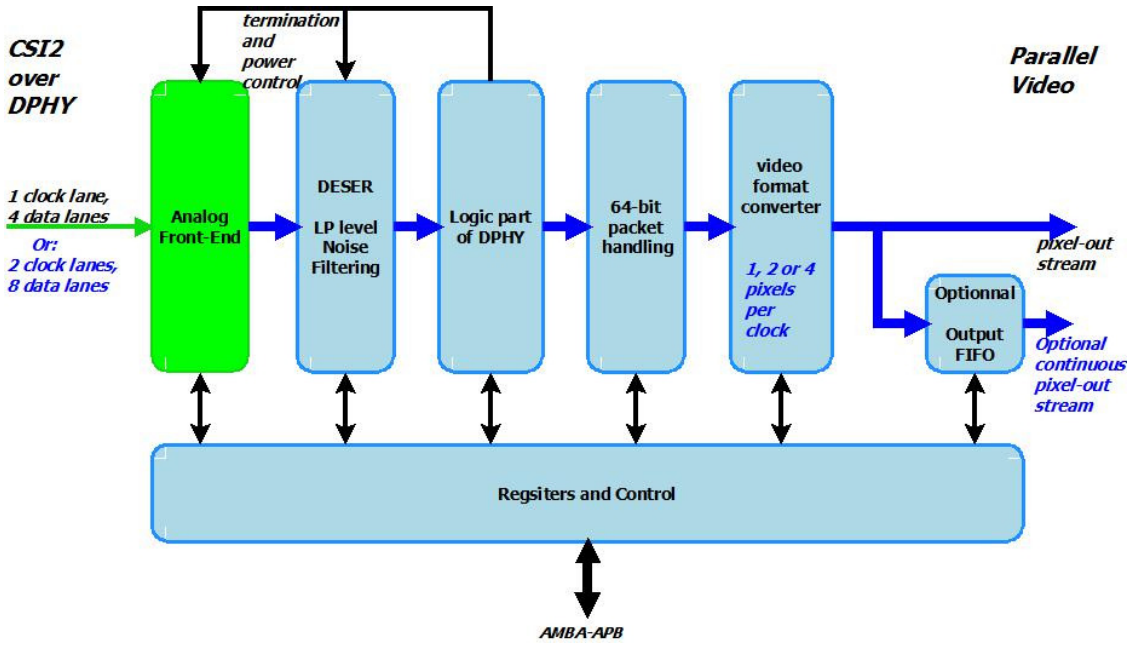
Application processor vendors also face speed issues. Processing frames of 16 million pixel at 60 fps require the processing of 1G pixel per second. As employing a 1GHz clock is not desirable, the trend is to process more than one pixel in each clock cycle.

The SVRPlus-CSI2-I IP Core Family

VLSI Plus' SVRPlus-CSI2-I family is designed to support those trends, and, at the same time, work with a relatively slow clock rate, processing several pixels per clock.

All SVRPlus-CSI2-I family members have an internal 64-bit bus. With this bus width, 10Gbps can be handled by a reasonable167MHz clock.

The output path of members of the SVRPlus-CSI2-I family can handle 1, 2 or 4 pixels in parallel. Image sensors which generate, for example, 12M * 60 fps = 720M pixels per second, can be handled by the SVRPlus-CSI2-I-X4 driven by a 180MHz clock



The SVRPlus-CSI2-I-4X can handle from 1to 4 data lanes. The SVRPlus-CSI2-I-8X , can handle up to 8 data lanes, with one or two clock lanes, and at up to 1.5Gbps per lane.

Functionality Highlights

The SVRPlus-CSI2-I family functionality highlights include:

- Configurable 1, 2, 3 or 4 data lanes (SVRPlus-CSI2-I-4X);
- Configurable 1 or 2 clock lanes; 1,2,3,4 or 8 data lanes (SVRPlus-CSI2-I-8X);
- 64 bit internal data bus
- 1 (SVRPlus-CSI2-I-X1), 2 (SVRPlus-CSI2-I-X2) or 4 2 (SVRPlus-CSI2-I-X4) pixels output per clock
- Up to 1.5Gbps per lane;
- All CSI2 functionality implemented in hardware, freeing the CPU to other tasks
- Support of all data formats.
- Extensive set of registers, accessible by AMBA APB bus
- Programmable timing parameters
- Optional support of CSI2 compressed-video formats
- Optional output FIFO for continuous output streams
- Optional Error counting hardware, for on-line BER measurements

Clock Rates and Performance

The SVRPlus-CSI2-I main clock frequency is set by the following constraint:

$$Min(Fclk) \geq 1.05*(max(bps/8, L*bps/64, PPS/P)$$

Where:

- bps is the maximum bit rate per lane;
- L is the number of lanes in use
- pps is the pixel-per-second rate of the image
- P is the number of pixels processed in parallel (1 of that option is not ordered

Here are two examples (we assume that video is active 95% of the time; that is – horizontal and vertical blank last 5% of the overall time):

1. **10 M-pixel sensor, 4 lanes, 30 fps, RAW12; SVRPlus-CSI2-I-X1 (1 pixel output per clock):**

pps = 10M * 30 / 0.95 = 316M

bps = 316M * 12 / 4 = 947M

Min(Fclk) ≥ 1.05*max(947M/8, 4*947M/64, 316M) = 331MHz

2. **12 M-pixel sensor, 8 lanes, 60 fps, RAW10; SVRPlus-CSI2-I-X4 (4 pixel output per clock)**

pps = 12M * 60 / 0.95 = 757M

bps = 757M * 10 / 8 = 947M

Min(Fclk) ≥ 1.05*max(947M/8, 8*947M/64, 757M/4) = 199MHz

For more information, please write to info@vlsiplus.com

Please visit our website at www.vlsiplus.com