4-Lane CSI2 Serial Video Transmitter With Basic Application Module for FPGA Implementations (SVT-CS4-AP1_F)

Data Sheet

Version 7, May 10, 2017

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Introduction and Overview

This document describes VLSI Plus (www.vlsiplus.com) basic-application 4 data lanes CSI2 Serial Video Transmitter (SVT-CS4-AP1) - a serial transmitter for single video stream, complying with MIPI® CSI2 standard.

The SVT-CS4 is VLSI Plus basic CSI2 transmitter IP core, designed to be embedded in CMOS Image Sensors, as well as in application processors. It supports a clock lane and from one to four data lanes. The SVT-CS4-AP1 adds a basic application core to the SVT-CS4, which results in a complete single video stream CSI2 transmitter.

MIPI® (Mobile Industry Processor Interface) is an industry consortium, which defines standards for the interface between modules of a mobile device. Two of those standards are D-PHY, defining the physical level of high speed communication, and CSI2, defining the Camera Serial Interface.

The SVT-CS4 supports MIPI®CSI2 over MIPI D-PHY.

SVT-CS4-AP1 Functionality highlights include:

- 1 clock lane, up to four data lanes[1]
- Simple interface – legacy parallel-video input, augmented by an Early-HD signal
- Supports all pixel formats, with up to 16 bit per pixel - RGB444, RGB555, RGB565, RAW8, RAW10, RAW12, RAW14, YUV420 (legacy, 8 bit, 10 bit), YUV422 (8 bit, 10 bit), and user-defined data formats.
- Uses simple off-IP analog PHY (clock and data lane modules)

[1] The maximum number of data lanes (from 1 to 4) is defined by the user when the IP is ordered. Lower number results in less silicon area. For a given maximum number of data lanes, the number of active lanes is defined in a configuration register, and can be changed when the device is reset.

The Analog Front-End

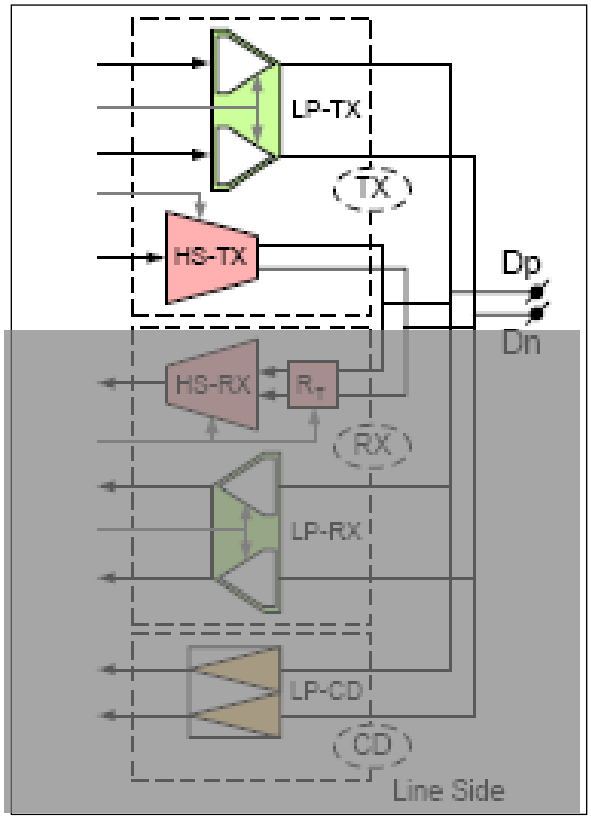

Figure 1: Analog PHY

Figure 1 depicts a block diagram of the analog part of MIPI D-PHY, per lane. The customer should add an off-FPGA analog front end, such as Meticom 20902, or a resistor-only DPHY-compatible analog front end, such as those suggested by various FPGA vendors

Simplified Block Diagram

A simplified block diagram of the SVT-CS4-AP1 is depicted in Figure 2. The SVT-CS4_AP1 comprises an Application Module 1 (APKG1), which varies according to the application, and an application-independent Generic Module. The combination of the generic core and the basic application core is designated SVT-CS4-AP1.

Generic Module Description

Parallel pixel is input from a parallel-output camera (designated 1 in the figure), and comprises 16 bit pixels. If video formats of less than 16 bits are used, the unused most significant bits are ignored. Incoming pixel stream is converted to packets in the data-path unit

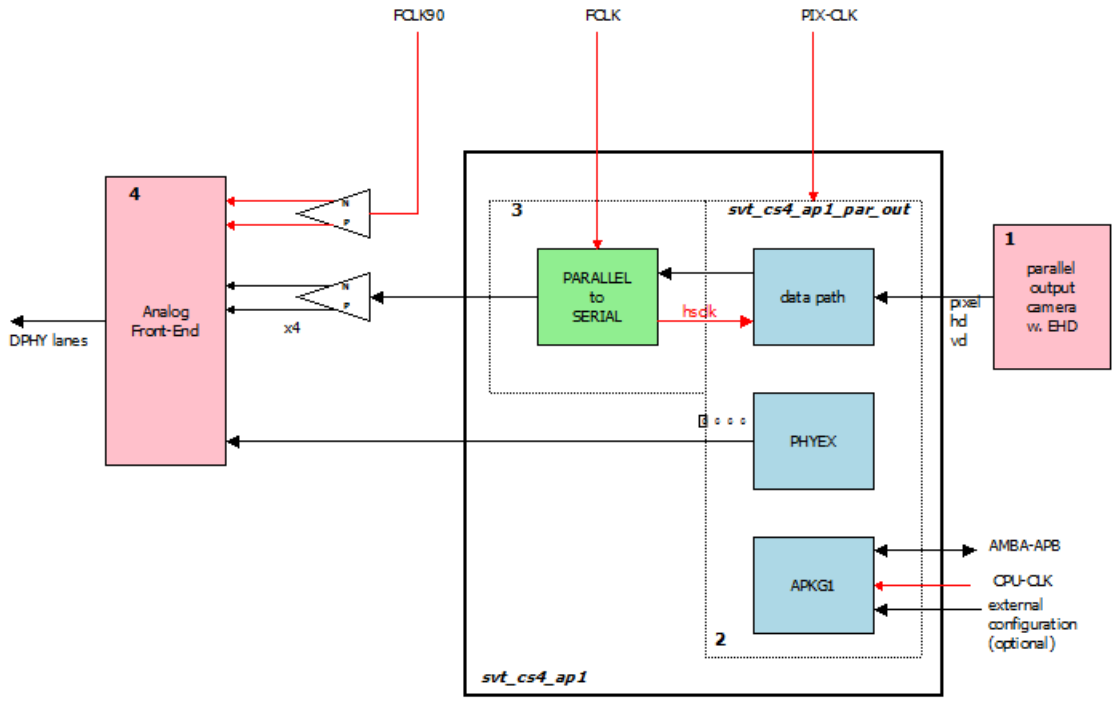

Figure 2: SVT-CS4-AP1 Block Diagram

The SVT-CS4-AP1 data path generates short and long packets, as defined by the Application Module APKG1. This Application Module facilitates a single video format, with constant packet parameters (except for the frame-number field, which increments automatically, and the packet length field, which changes between odd and even lines in YUV420). Other application modules offered by VLSI Plus change the parameters between packets, allowing interleaving of, for example, JPEG and live video output.

A CSI2-Protocol block (not shown) controls the PHYEX, which, in turn, controls the Analog Front End, which drives the clock and data lanes.

Control bits v_clk_stop and h_clk_stop, driven by APKG1, indicate whether the SVT-CS should deactivate the clock lanes between frames (v_clk_stop) and between lines (h_clk_stop). It is the programmer responsibility to make sure that horizontal and vertical blank periods are sufficiently long to allow horizontal and vertical clock stop periods. (A User Reference Excel sheet is provided, to help the user program all the parameters).

The PHYEX implement the digital functions of the D-PHY as defined by MIPI, including packet start-end protocols, sync codes, and more. The PHYEX directly generates the low-power clock-lane and data-lane signals, which are subsequently level-shifted to DPHY specifications by the Analog Front-End.

High speed parallel to serial circuits (designated 3), one for each data lane, are used to convert the incoming HS bytes to a serial stream of bits.

The Analog Front End (designated 4) typically comprises high speed differential drivers, as well as low-power slew-rate-controlled CMOS drivers.

Note:

- The blocks encompassed by dotted-line rectangle 2 are part of a sub-module named svtcs_cs4_ap1_par_output.
- If the External Configuration option is ordered, the configuration registers are external to the IP (this may be useful if the customer wishes to change configuration during the video frame)
- For low data rates (typically less than 1Gbps per lane) parallel to serial module 3 can be implemented by RTL. A simple serializer module is provided for that purpose with the IP. For higher speed, the customer should embed an IO-bound serializer using FPGA IO customization tools (such as Xilinx selectio)

Clocks

An off-IP PLL should be embedded, providing four clock sources:

- pix_clk – pixel clock; used to drive pixels from the camera to the IP, and between internal units of the IP
- cpu_clk – used to read-write the IP registers. Mus be at least x3 slower than pix_clk
- FCLK and FCLK90 - fast clock at ½ the lane bit rate. FCLK90 lags FCLK by 90 degrees

The serializer divides FCLK by 4 to generate the byte sampling clock, designated HSCLK

Off-IP FIFO

As described above, an EHD – Early HD – signal must precede the HD and the accompanying pixels input from the camera. Many cameras have an internal indication prior to the start of the video stream, which can be used for that. In other cases, the user may need to use HD as EHD, and then assert a delayed video stream to the camera input of the SVT-CS, along with a delayed HD.

The delaying of the video stream requires a FIFO, which can be added by the customer, or provided as an IP option.

SVT-CS4-AP1-F Module Pads

The following table comprises the full list of the SVT-CS4-AP1-F (including the serializer) pads.

Symbol	Dir	Description
Connection to Analog Front-End		
clk_lp_dp	O	Clock lane lp level positive signal.
clk_lp_dn	O	Clock lane lp level negative signal
clk_hs_bit	O	Clock lane hs level
clk_en_hs	O	Enable clock lane HS mode
clk_en_lp	O	Enable clock lane LP mode
data_lp_dp[3:0]	O	Data lanes lp level, positive signal.
data_lp_dn[3:0]	O	Data lanes lp level negative signal
data_hs_bit[3:0]	O	Data lanes hs level signal
data_en_hs[3:0]	O	Enable data lanes HS mode
data_en_lp[3:0]	O	Enable data lanes LP mode
force_clk_hs0	O	force the clock lane to HS0 (not needed for 20902 analog front end)
Clock and Reset		
pix_clk	In	Transmission Clock; used to sample incoming pixels
cpu_clk	In	Used to write data into the SVT-CS4-AP1 registers (AMBA-APB pclk). must be at least 3 times slower then pixel_clock
fclk	In	Bit clock. Equal exactly m/(n*2) times pixel-clock frequency, where m is the number of bits per pixel, and n is the number of active data lanes
fclk_90	In	Second bit clock; lags fclk by 90 degrees

Symbol	Dir	Description
Video Input Bus (sampled at pix_clk low to high transition)		
Pixel[15:0]	In	Pixel Bus
HD	In	Horizontal Drive. Encompasses exactly all pixels in a video line
EHD	In	Early HD. Used by the SVT-CS4-AP1 to initiate a long packet. Precedes the HD leading edge by at least 2 clocks (See Programmer Reference Manual). Trailing edge should trail HS leading edge by at least 0 UI. . See Programmer-Reference Excel-sheet
VD	In	Vertical Drive. Used by the SVT-CS4-AP1 to generate FS and FE pulses. VD leading edge should precede the first EHD by a time interval which should be sufficient for sending an FS short packet (see Programmer Reference Excel Sheet). VD trailing edge can coincide or lag after the trailing edge of the last HD in the frame.
AMBA APB Bus		
Pselx	In	AMBA APB Select.
Penable	In	AMBA APB Enable.
Paddr[7:2]	In	AMBA APB Address; selects one of sixteen 32 bit registers.
SVT_reset_n	In	AMBA APB ~reset.
Pwdata[31:0]	In	AMBA APB write-data.
SVR_Prdata[31:0]	Out	AMBA APB read-data.
Pwrite	In	AMBA APB Write

Note: when the customer generates an IO-bound fast serializer using FPGA specific tools, more pads may be needed for calibration, as defined by the serializer generation tool.

The following table comprises the full list of the SVT-CS4-AP1-PAR-OUT, which is instantiated in the svt-cs4-ap1 module.

Symbol	Dir	Description
Connection to Analog Front-End		
clk_lp_dp	O	Clock lane lp level positive signal.
clk_lp_dn	O	Clock lane lp level negative signal
clk_en_hs	O	Enable clock lane HS mode
clk_en_lp	O	Enable clock lane LP mode
data_lp_dp[3:0]	O	Data lanes lp level, positive signal.
data_lp_dn[3:0]	O	Data lanes lp level negative signal

Symbol	Dir	Description
data_en_hs[3:0]	O	Enable data lanes HS mode
data_en_lp[3:0]	O	Enable data lanes LP mode
Connection to Serializer		
hsb1[7:0]	O	lane 1 HS byte
hsb2[7:0]	O	lane 2 HS byte
hsb3[7:0]	O	lane 3 HS byte
hsb4[7:0]	O	lane 4 HS byte
Clock and Reset		
hsclk	In	byte sampling clock, from the serializer
pix_clk	In	Transmission Clock; used to sample incoming pixels
cpu_clk	In	Used to write data into the SVT-CS4-AP1 registers (AMBA-APB pclk). must be at least 3 times slower then pixel_clock
fclk	In	Bit clock. Equal exactly m/(n*2) times pixel-clock frequency, where m is the number of bits per pixel, and n is the number of active data lanes
fclk_90	In	Second bit clock; lags fclk by 90 degrees
Video Input Bus (sampled at pix_clk high to low transition)		
Pixel[15:0]	In	Pixel Bus
HD	In	Horizontal Drive. Encompasses exactly all pixels in a video line
EHD	In	Early HD. Used by the SVT-CS4-AP1 to initiate a long packet. Precedes the HD leading edge by at least 2 clocks (See Programmer Reference Manual). Trailing edge should trail HS leading edge by at least 0 UI. . See Programmer-Reference Excel-sheet
VD	In	Vertical Drive. Used by the SVT-CS4-AP1 to generate FS and FE pulses. VD leading edge should precede the first EHD by a time interval which should be sufficient for sending an FS short packet (see Programmer Reference Excel Sheet). VD trailing edge can coincide or lag after the trailing edge of the last HD in the frame.
AMBA APB Bus		
Pselx	In	AMBA APB Select.
Penable	In	AMBA APB Enable.
Paddr[7:2]	In	AMBA APB Address; selects one of sixteen 32 bit registers.
SVT_reset_n	In	AMBA APB ~reset.
Pwdata[31:0]	In	AMBA APB write-data.
SVR_Prdata[31:0]	Out	AMBA APB read-data.

Symbol	Dir	Description
Pwrite	In	AMBA APB Write

Assignment of Pixel input pads

In all RAW formats, only the LS bits of the PIXEL input pins are used; for example, in RAW12, bits 11:0 of the video input are connected to pads PIXEL[11:0], and pads PIXEL[15:12] are connected to zero or one (ignored)

In other formats, pad wiring is as depicted in the CSI2 specifications. For example, for RGB555:

- Red[4:0] is connected to PIXEL[15:11];
- Green[4:0] is connected to PIXEL[10:6];
- Blue[4:0] is connected to PIXEL[4:0]
- PIXEL[5] input is ignored (the IP will send 0 in the packet)

Timing Waveforms

The waveforms of the SVT-CS4-AP1 are depicted in Figure 3. Input is synchronized to Pixel-Clock. Detection of a VD leading edge initiates an FS short packet. AHD starts a Long Packet header. Data for the long packet is sampled from the video-input bus when HD is active. When the last pixel is received, as indicated by HD trailing edge, the SVT-CS4-AP1 adds Footer, and terminates the packet. Note that in the SVT-CS4-AP1 the length of HD must agree with the WC field of the LP header (see chapter on LP_Header_Reg below)

The trailing edge of VD, which must occur after the last pixel has been sampled, triggers an FE short packet.

Between packets, the data lanes enter LP state. The clock lane may enter LP state between frames and/or between lines, or may toggle at all times – see discussion above.

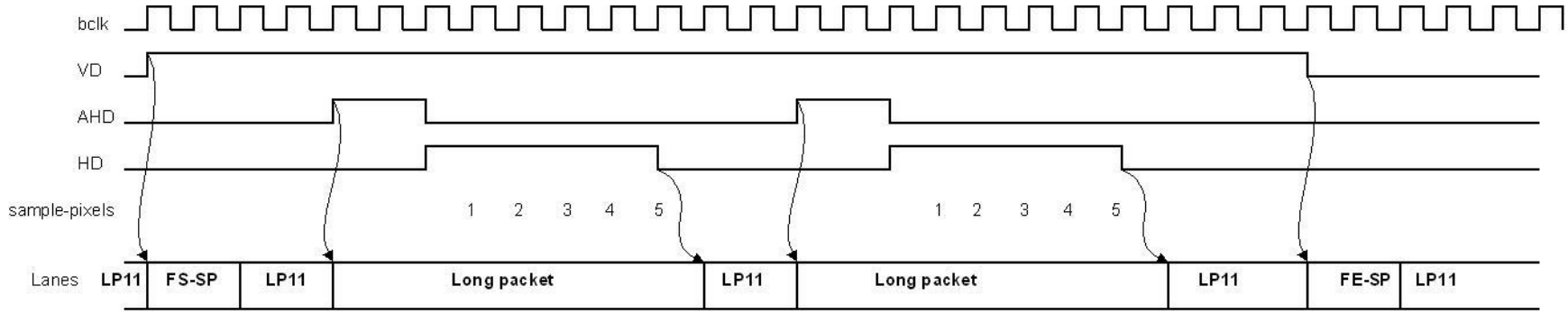

Figure 3: Waveforms

Continuous and Non-Continuous Clock-Modes

CSI-2 specifications define continuous and non-continuous clock modes. While in Continuous Clock Mode, the clock lane is always at High Speed (HS) Toggle state. While in non-continuous clock-mode, the clock lane may switch to Low Power (LP) state between packets, following a timed sequence as defined in the DPHY specifications.

The SVT-CS4-AP1 supports continuous clock mode and three types of non-continuous clock modes – vertical-clock-stop, where the clock lane switches to LP state only between video frames; horizontal-clock-mode, where the LP state is assumed between video lines, and a mode where LP state is entered between video lines and between video frames.

The mode is configured by bits 5 and 6 of the SVT_Cfg_Reg:

- Bits [6:5] = 00: continuous clock mode
- Bits [6:5] = 10: non-continuous clock mode; clock lanes switches to LP state between video frames
- Bits [6:5] = 11: non-continuous clock mode; clock lanes switches to LP state between video frames and between video lines
- Bits [6:5] = 01: non-continuous clock mode; clock lanes switches to LP state between video lines but not between video frames (note – this last mode is not a practical choice – gaps between lines are typically much shorter than gaps between frames)

Switching between continuous and non-continuous clock modes

Changing the continuous-clock-mode configuration, as well as changing other bits of the SVT_Cfg_Reg, should be done when there is no video. Failure to do so may result in a single corrupt video frame.

There are CSI2 receivers which may operate in continuous and non-continuous clock modes without any settings - when a clock lane goes through the sequence LP11-LP01-LP00-HS0 and HS-toggle, the termination will be connected (when the lane is at LP00) and the clock lane will be in HS-toggle mode. The clock lane will then continue toggling if in continuous clock mode, or stop between packets if in non-continuous clock mode – the receiver will function properly in both cases.

However, there are also CSI2 receivers which support continuous clock-mode only. Those receivers may have a fixed100 ohm termination on the clock lane. When a CSI2 Transmitter is connected to such receiver, it is undesirable to go through LP01 state, as a strong current will flow between the Dp and Dn wires of the clock lane, through the 100-ohm termination.

To support receivers with constant-on termination, the SVT_Cfg_Reg should be programmed to continuous-clock-mode when SVT_en register is at 0. The Dp and Dn wires of the clock lane (and all other lanes) are at LP00 when SVT_en is at 0. When

SVT_en will be set to 1, the clock lane will go directly to HS-toggle; thus no excessive current will ever flow between the Dp and Dn wires.

To support CSI2 receivers with switchable clock-lane termination, the user should follow the sequence:

1. SVT_en is 0. The clock lane and all other lanes are at LP00
2. SVT_Cfg_Reg is set to one of the non-continuous clock modes. No change occurs in the lanes
3. SVT_en is set to 1. Now the clock lane will assume LP11, waiting for a video frame
4. If SVT_Cfg_Reg is set to continuous-clock-mode before video is active, the clock lane will go through the sequence LP01-LP00-HS0-HS-Toggle.

Registers

There are 13 32-bit registers in the SVT-CS4-AP1. The list of registers is given below.
Note: Bits that are marked as “Reserved” or are not mentioned will be read as 0.

Here is the list of all registers, with their addresses:

ADDRESS	NAME	FUNCTION
0x00	SVT_En_Reg	Enable SVR operation
0x10	SVT_Cfg_Reg	General Configuration
0x14	SVT_Timer_CFG_A_Reg	Programmable timing parameters, set A
0x18	SVT_Timer_CFG_B_Reg	Programmable timing parameters, set B
0x1C	SVT_Timer_CFG_C_Reg	Programmable timing parameters, set C
0x20	Last_Frame_Count_Reg	Controls the last frame number to be inserted in FS and FE short packets before it is reset to 1
0x24	FS_Header	32 bit header for FS short-packet
0x28	FE_Header	32 bit header for FE short-packet
0x2C	LP_Header	32 bit header for long packets
0x30*	Forced_Format	Sets the video format to be used
0x34*	Force_Lanes_Reg	Facilitates forcing lane state, for testing
0x38*	SOT_Control_Reg	Facilitates insertion of SOT errors
0x3C*	ECC_Control_Reg	Facilitates insertion of ECC errors
0x40*	CRC_Control_Reg	Facilitates insertion of CRC errors
0x80	Status_Reg	Indicates the status of the SVT; used for debug
0xF8	IP Vendor	The MIPI-assigned vendor code for VLSI Plus
0xFC	Version	Unique 32 bit code

*: Implemented if the DEBUG option of ordered

The next sections will elaborate on each of the registers.

SVT_En_Reg

This register enables the operation of the SVT. If it is not set, the SVT idles, and the lanes are at LP11.

Type: Command/Configuration
Access: Write/Read
Address: 8'h00
Contents:

Bit	Name	Description	Default Value
0	SVT_En	This bit enables & disables the activity of the SVT. 0 – SVT is disabled. 1 – SVT is enabled.	0
31:1	Reserved		

SVT_CFG

This register is the main configuration register of the SVT.

Type: Configuration
Access: Write/Read
Address: 10
Contents:

Bit	Name	Description	Default Value
2:0	Reserved		
4:3	Lanes	Number of data lanes: 00: 1 data lane; 01: 2 data lanes; 10: 3 data lanes; 11: 4 data lanes	0x0

Bit	Name	Description	Default Value
5	H_clk_stop	Stop the clock lanes between lines	0x0
6	V_clk_stop	Stop the clock lanes between frames	0x0
7	Auto-Increment	Auto-increment the frame number field in FS and FE. If set, frame number will increment between frames, and reset to 1 when the value indicated in the last_frame_count is reached.	0x1 (increment)
8	Enter ULPS	If this bit is set, the SVT will send ULPS sequence on all channels, and set the lanes to LP00. Note – Writing 1 to this register should be preceded by writing 0xFFFFFFFF to the Force_Lanes_Reg Note – in order to exit ULPS for some or all lanes, do the following: 1. Force the applicable lanes to LP00 (see section on Force_Lanes_Reg) 2. Write 0 to bit 8 of the SVT_CFG register 3. Force the applicable lanes to LP10 (see section on Force_Lanes_Reg) 4. Wait at least 1 ms 5. Unforce the applicable lanes (see section on Force_Lanes_Reg) Note: ULPS Entry code will be signaled in al lanes, even if not all lanes are configured.	0x0
31:9	Reserved		0x00

SVT_Timer_Cfg_A_Reg

This register holds the configuration numbers for several hardware timers. Units are pixel-clock periods.

Type: Configuration
Access: Write/Read
Address: 0x14
Contents:

Bit	Name	Description	Default Value
7:0	Tlpx	Timeout counter for Tlpx, Tclk-post, Tclk-pre and Tclk-prepare. See DPHY Specification and the SVT-CS4AP1 Programmer Reference Manual	0x32
15:8	Tclk-post		0x40
23:16	Tclk-pre		0x8

Bit	Name	Description	Default Value
31:24	Tclk-prepare		0x30

SVT_Timer_Cfg_B_Reg

This register holds the configuration numbers for several hardware timers. Units are pixel-clock periods.

Type: Configuration
Access: Write/Read
Address: 0x18
Contents:

Bit	Name	Description
7:0	Tclk-trail	Parameters are defined in MIPI® DPHY specifications. Programming guidance can be found in the SVT-CS4AP1 Programmer Reference Manual.
15:8	Tclk-zero	
23:16	Ths-prepare	
31:24	Ths-trail	

SVT_Timer_Cfg_C_Reg

Type: Configuration
Access: Write/Read
Address: 0x1C
Contents:

Bit	Name	Description	Default Value
9:0	Tsync-hold-SP	Time to delay HS sync code from VD rising edge (FS) or falling edge (FE), in pix-clk units. Includes the periods Tlpx, Ths-prepare, which are defined separately, and Ths-zero, which is indirectly defined here. Programmed value should guarantee min Ths-prepare + Ths-zero	100
31:10		Not used	

This register holds the configuration value for Tsync-hold-SP, in units of pix-clk, for short packets.

Notes: this value is applicable to short packets only. For long packets, the lead time of EHD relative to HD determines the value of DPHY parameter $T_{hs\text{-}prepare}$ + $T_{hs\text{-}zero}$, and $T_{hs\text{-}prepare}$ is set in SVT_TIMER_CFG_B_REG.
Note – the value of this parameter will never be less than 5 pix-clk + 4 hs-sclk + sync uncertainty (1-2 hs-clk pulses), even if this register is programmed with a lower value. To be effective, the programmed value should be loner than Tlpx+ths-prepare+ths-zero +5pix_clk + 4hsclk

Please refer to the Programmer Reference Guide.

Last_Frame_Count_Reg

Last frame count before resetting to 1 (Applicable only if Auto-Increment is set in SVT_CFG register)

Type: Configuration
Access: Write/Read
Address: 0x20

Contents:

Bit	Name	Description	Default Value
15:0	Last_Frame_Count	the last frame count indicated in the FS and FE frame-number fields before it is reset to 1	0x100
31:16	Not used		

FS_Header_Reg

The content of this register is used as a header when a FS short packet is transmitted.
Type: Configuration
Access: Write/Read
Address: 0x24

Contents:

Bit	Name	Description	Default Value
5:0	DT	Data Type field. Must be '000000' according to CSI	0x00
7:6	VC	Virtual Channel. See CSI specifications	0x0
23:8	Data	Data Field. Auto-increments if the corresponding bit in CFG_Reg is set.. Note – if the AI bit of CFG_Reg is not set, the value of the Data field must equal 0x00 in order to comply with CSI2 specifications	0x0000
31:24	Not used	ECC is calculated by the IP hardware; this field is not needed	

FE_Header_Reg

The content of this register is used as a header when a FE short packet is transmitted.
Type: Configuration
Access: Write/Read
Address: 0x28

Contents:

Bit	Name	Description	Default Value
5:0	DT	Data Type field. Must be '000001' according to CSI	0x01
7:6	VC	Virtual Channel. See CSI specifications. Should match the VC field of FS_Header_Reg	0x0
23:8	Data	Data Field. Auto-increments if the corresponding but in CFG_Reg is set. Note – if the AI bit of CFG_Reg is not set, the value of the Data field must equal 0x00 in order to comply with CSI2 specifications	0x0000
31:24	Not used	ECC is calculated by the IP hardware; this field is not needed	

LP_Header_Reg

The contents of this register are used as a header when a long packet, carrying a video line, is transmitted.

Type: Configuration
Access: Write/Read
Address: 0x2c

Contents:

Bit	Name	Description	Default Value
5:0	DT	Data Type field, indicating the video format (see CSI specifications)	0x2A (RAW8)
7:6	VC	Virtual Channel. See CSI specifications. Should match the VC fields of FS_Header_Reg, FE_Header_Reg	0x0
23:8	WC	Word-Count – number of bytes in the packet***. Must divide by 8*** Note: in YUV420, WC field should contain the length of the odd lines. The number for even lines will be automatically generated.	
31:24	Not used	ECC is calculated by the IP hardware; this field is not needed	

Forced_Format_Reg

This register is useful for testing full CSI2 link functionality. It is implemented only if the DEBUG option is ordered

This register defines the data type to be used when packing the pixels into bytes. According to CSI2 specifications this format must equal the DT field of the LP Header. It is the programmer's responsibility to assign the same value to this register and to the DT field of the LP_Header_Reg when normal CSI2 operation is carried out.

Type: Configuration
Access: Write/Read
Address: 0x30

Contents:

Bit	Name	Description	Default Value
5:0	DT	Data Type field, indicating the video format (see CSI specifications)	0x2A (RAW8)
31:6	Not used		

Force_Lanes_Reg

This register is useful for testing full CSI2 link functionality. It is implemented only if the DEBUG option is ordered

This register is used for testing of the DC levels of the analog PHY. It forces lanes to a specified state.

The register should be set to 0xFFFFFFFF to allow the Application Package to force the lanes into ULPS entry sequence.

Type: Configuration
Access: Write/Read
Address: 0x34
Contents:

Bit	Name	Description	Default Value
1:0	Reserved		0x0
2	Force_clk_LP	Clock lane is forced to LP mode	0x0
3	Clk_Dp_LP	The LP state to which the Dp line of the Clock lane is forced	0x0
4	Clk_Dn_LP	The LP state to which the Dn line of the Clock lane is forced	0x0
7:5	Reserved		0x0
8	Force_lane1_LP	data lane 1 is forced to LP mode	0x0
9	Lane1_Dp_LP	The LP state to which the Dp line of data lane 1 is forced	0x0
10	Lane1_Dn_LP	The LP state to which the Dn line of data lane 1 is forced	0x0
13:11	Reserved		0x0
14	Force_lane2_LP	data lane 2 is forced to LP mode	0x0
15	Lane2_Dp_LP	The LP state to which the Dp line of data lane 2 is forced	0x0
16	Lane2_Dn_LP	The LP state to which the Dn line of data lane 2 is forced	0x0
19:17	Reserved		0x0
20	Force_lane3_LP	data lane 4 is forced to LP mode	0x0
21	Lane3_Dp_LP	The LP state to which the Dp line of data lane 4 is forced	0x0
22	Lane3_Dn_LP	The LP state to which the Dn line of data lane 4 is forced	0x0
25:23	Reserved		0x0
26	Force_lane4_LP	data lane 4 is forced to LP mode	0x0
27	Lane4_Dp_LP	The LP state to which the Dp line of data lane 4is forced	0x0
28	Lane4_Dn_LP	The LP state to which the Dn line of data lane 4 is forced	0x0
31:29	Reserved		0x0

SOT_Control_Reg

This register is useful for testing full CSI2 link functionality. It is implemented only if the DEBUG option is ordered

The register controls insertion of SOT errors in the stream. When a SOT error is inserted, a specified bit of the 16 bit sync code (B8) is inverted.

SOT error can be defined for the SOF short packet, the EOF short packet, and the first long packet in the frame. Separate control for the four lanes is provided

Type: Configuration
Access: Write/Read
Address: 0x38
Contents:

Bit	Name	Description	Default Value
0	FS_SOT_L1	Insert FS SOT error in Lane 1	0x0
1	FE_SOT_L1	Insert FE SOT error in Lane 1	0x0
2	LP_SOT_L1	Insert LP SOT errors, Lane 1, on the first video lines of the frame	0x0
6:3	Flipped bit L1	Bit to flip (M.S. bit is 15), Lane 1	0x0
8	FS_SOT_L2	Insert FS SOT error in Lane 2	0x0
9	FE_SOT_L2	Insert FE SOT error in Lane 2	0x0
10	LP_SOT_L2	Insert LP SOT errors, Lane 2, on the first video lines of the frame	0x0
14:11	Flipped bit L2	Bit to flip (M.S. bit is 15), Lane 2	0x0
16	FS_SOT_L3	Insert FS SOT error in Lane 3	0x0
17	FE_SOT_L3	Insert FE SOT error in Lane 3	0x0
18	LP_SOT_L3	Insert LP SOT errors, Lane 3, on the first video lines of the frame	0x0
22:19	Flipped bit L3	Bit to flip (M.S. bit is 15), Lane 3	0x0
24	FS_SOT_L4	Insert FS SOT error in Lane 4	0x0
25	FE_SOT_L4	Insert FE SOT error in Lane 4	0x0
26	LP_SOT_L4	Insert LP SOT errors, Lane 4, on the first video lines of the frame	0x0
30:27	Flipped bit L4	Bit to flip (M.S. bit is 15), Lane 4	0x0

ECC_Control_Reg

This register is used for testing full CSI2 link functionality. It is implemented only if the DEBUG option is ordered

The register controls insertion of ECC errors in the stream

Type: Configuration
Access: Write/Read
Address: 0x3C
Contents:

Bit	Name	Description	Default Value
4:0	FS_ECC_bit_flip	Bit to flip in FS header (00000➔no flip)	0x00
5	FS_ECC_HE	Force HE in FS header	0x0
10:6	FE_ECC_bit_flip	Bit to flip in FE header (00000➔no flip)	0x00
11	FE_ECC_HE	Force HE in FE header	0x0
16:12	L1_ECC_bit_flip	Bit to flip in video line 1 header (00000➔no flip)	0x00
17	L1_ECC_HE	Force HE in video line 1 header	0x0
22:18	L3_ECC_bit_flip	Bit to flip in video line 3 header (00000➔no flip)	0x00
23	L3_ECC_HE	Force HE in video line 3 header	0x0
28:24	L4_ECC_bit_flip	Bit to flip in video line 4 header (00000➔no flip)	0x00
29	L4_ECC_HE	Force HE in video line 4 header	0x0

Note about bit-to-flip – if any number 0<n<32 is specified in this field, the value of bit (n) of the header's [31:0] bits will be flipped. If n=0 not bit will be flipped, and bit 0 cannot be flipped.
Note about forcing HE: when this bit is set, bits 0 and 31 of the header will be flipped.

CRC_Control_Reg

This register is used for testing full CSI2 link functionality. It is implemented only if the DEBUG option is ordered

The register controls insertion of CRC errors in the stream. A single CRC error can be inserted in any of the first 32 video lines

Type: Configuration
Access: Write/Read
Address: 0x40
Contents:

Bit	Name	Description	Default Value
n (n=0…31)	CRC_ERROR[n]	Insert CRC error in all lines for which the corresponding bit is set. For this purpose line counting starts at 0 For example, n=32'h01010101 will result in CRC errors in lines 0, 8, 16, 24. If n=0 no CRC error will be inserted	0x0

Status_Reg

This register can be used to read the status of the SVT-CS4-AP1

Type: Debug
Access: Read/Write
Address: 0x80
Contents:

Bit	Name	Description
2:0	Status	000: the SVT is idle 001: the SVT is sending an FS SP 010: the SVT is sending an FE SP 011: the SVT is sending a LP 100: the SVT is sending ULPS-Entry command 101: the SVT is un ULPS mode
31:3	Not used	

The register is cleared by writing 0x00000000 to address 0x80

IP_Vendor

Read-Only register, containing the unique vendor code assigned to VLSI Plus by the MIPI consortium.

Type: Static status
Access: Read-only
Address: 0xFC
Contents: 0x00000206

Version

Version Read-Only register. It has a unique code for the version of the current release, and will be updated when new versions of the SVT-CS4-AP1 are released.

Type: Static status
Access: Read-only
Address: 0xFC
Contents: unique 32 bit code

Ordering Options

When placing an order for the SVT-CS4-AP1, the customer should specify options as detailed below:

Maximum number of data lanes

The customer can specify any number from 1 to 4. A larger number implies higher silicon area.

DEBUG Option

As described in the registers chapter, some of the SVT-CS4-AP1 registers can be programmed to inject communication errors, to test for SVT-SVR link error handling features.

Input FIFO

For cameras which do not generate an EHD signal preceding the HD, an input FIFO is needed, to delay the incoming video stream and the HD (in this case, the non-delayed HD output of the camera will be used as EHD).

This FIFO can be added by the customer or provided as an optional addition to the SVT-CS4AP1 IP.

I2C to AMBA Bridge

It is possible to add an I2C to AMBA Bridge, to allow serial access to all registers.

Registers Default Values

In order to simplify or even eliminate the initialization process, the customer may specify the reset values of all registers

External Configuration

It is possible to set the configuration by means of external inputs rather than AMBA-APB accessible registers. When this option is ordered, more pads are added to the IP. Please contact VLSI Plus for details.,