1 to 4 Lane
Serial Video Transmitter
For MIPI CSI2
(SVT-CS4AP1)

Information Brief

Introduction

This document is a short description of VLSI Plus (www.vlsiplus.com) 4 data lane CSI2 Serial Video Transmitter (SVT-CS4AP1) – a CSI serial transmitter for video streams.

The SVT-CS4AP1 comprises two parts:

- The SVTCS4L-Core- a generic SVT-CS2 transmitter, which can be used in a variety of applications, when coupled with various Application Modules
- The SVTCS_APP_MDL_1 - a simple application module supporting all non-multiplexed video transmission

The SVT-CS4AP1 is designed to interface smoothly with commonly used CMOS Image Sensors.

The number of supported data lanes is defined by the customer with the order. VLSI Plus then compiles the RTL code with the appropriate compilation switches, and the customer gets a design optimized for his needs.

Overview

MIPI® (Mobile Industry Processor Interface) is an industry consortium, which defines standards for the interface between modules of a mobile device. Two of those standards are D-PHY, defining the physical level of high speed communication, and CSI2, defining the Camera Serial Interface.

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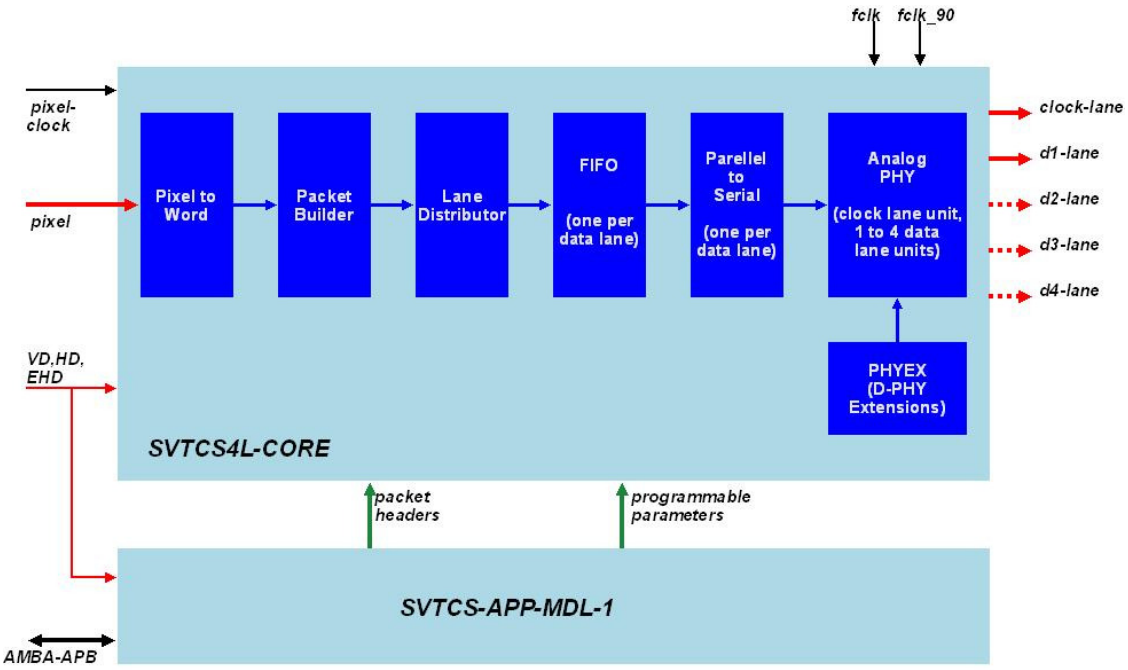
The SVT-CS4AP1 supports MIPI CSI2 over MIPI D-PHY.

Functionality highlights include:

- One clock lane, and one to 4 data lanes
- Up to 1Gbps per lane;
- Supports CSI2 RAW8, RAW10, RAW12, all YUV420, all YUV422 and User-Defined 8-bit formats (other CSI2 standards available as an option).
- CRC and ECC generation
- Programmable timing parameters

Simplified Block Diagram



The figure above depicts a simplified block diagram of the SVT-CS4-AP1.

The block marked ***SVTCS4L-CORE*** converts pixels to 16-bit words, generates complete packets by adding a header and a CRC footer, distributes data between the available lanes and controls the analog PHY according to the MIPI D-PHY specification.

The SVTCS4L-CORE, of less than 5000 gates (for one data lane, excluding the analog part) is a bare core without any registers. It comprises the basic hardware for the generation of CSI2 images, for a variety of applications. In the SVT-CS4AP1, a basic application package – the SVTCS-APP-MDL-1 is added to the basic core.

The ~3500 gates SVTCS-APP-MDL-1 incorporates registers, which hold configuration and timers settings, as well as basic logic. The registers are accessed through an AMBA-APB bus.

The image sensor should send parallel video stream, in one of the following CSI2 defined standards: Legacy YUV420-8b, YUV420-8 bit, YUV420-10 bit, YUV420-8bit CSPS, YUV420-10 bit CSPS, YUV422 8-bit, YUV422 10 bit, RAW8, RAW10, RAW12 or user-defined 8-bit (e.g. JPEG). The pixel stream is accompanies by standard HD and VD signals. In addition, an EHD (Early HD) pulse should be generated, so that the SVT could start the packet initiation process before the first pixel arrives from the sensor (EHD usually saves a FIFO – various image sensors can typically use the internal horizontal counters to generate such pulse early enough before the first pixel is output).

The user's circuit should also provide FCLK and FCLK_90 signals. FCLK is a high speed DDR clock toggling at the required bit rate (that is, 500MHz for 1GBPS). FCLK_90 lags FCLK by 90 degrees. FCLK and FCLK_90 are typically generated by a PLL, which also generates the PIXEL_CLK. The relationship between FCLK and PIXEL_CLK frequencies should follow the following equality:

$$F_{fclk} * L = 2 * F_{pclk} * BPP$$

Where:

- F_{fclk} – frequency of the FCLK and FCK_90 clock signals
- F_{pclk} – frequency of the pixel-clock signal
- L – number of active data lanes
- BPP – bit per pixel in the currently active video format (must be 8, 10 or 12)

Hard Core and Soft Core

The SVT-CS4AP1 comprises a process independent RTL soft core, and a process dependant hard core for the analog part of the PHY.

The user may choose to move the Parallel to Serial block to the hard-core, especially if the process technology is slow. However, for process technologies of 130nm and below the Parallel-to-Serial block easily synthesizes at 1Gbps (500MHz). The other parts of the SVT-CS4AP1 operate at pixel-clock, which is much slower.