SVRPlus-CSI2-Trial Version

Experience our top-of-the-line MIPI™ – CSI2 v2.0 Rx IP core – FOR FREE!

This Trial version is a sub-set of the SVRPlus-CSI2-F IP core, except that it is limited to 4 data-lanes, and some of the Options are omitted:

- ***Configurable 1 to 4 data lanes***
- ***Up to 800Mbps per lane with the supplied RTL de-seriallizer***
- ***Add you own IO-bound de-seriallizer (e.g. select-IO) for 1.5Gbps and beyond***
- ***AMBA-APB accessible registers***
- ***Support of all primary and secondary data formats.***
- ***64-bit internal data bus, for high throughput***
- ***Selectable output width: 1, 2 or 4 pixels per clock (compilation switch)***
- ***VCX support (up to 16 virtual channels)***

NOTE - the Trial version occasionally posts a TRIAL VERSION message reminder on the screen.

Load the SVRPlus-CSI2-FPGA datasheet from our website. You may be able to operate the IP with no support. If you are not sure, get the email/SKYPE™ support package for $200 – any time, and get a 48-hour support for 3 months

Good Luck!