4 input

CSI2 Video Multiplexor

(CSI2MUX-A1F)

for

FPGA implementation

Information Brief

Introduction

This document is a short description of VLSI Plus (www.vlsiplus.com) CSI2 multiplexing transceiver IP core for FPGA implementations - the CSI2MUX-A1-F.

The CSI2MUX-A1-F connects to 4 CSI2 cameras, multiplexes the video streams, and sends out a multiplexed CSI2 stream, where each camera input is assigned a different Virtual Channel.

The CSI2MUX-A1-F comprises modified versions of two VLSI Plus' IP cores, and glue logic. The two IP cores are:

- 1 to 4 instantiations of VLSI SVR-CSI-4 Serial Video Receivers;
- 1 instance of VLSI Plus SVT-CS4-AP2 Multiplexing Serial Video Transmitter core, modified and optimized.

For optimal usage of FPGA resources, the user is provided with compilation switches, which determine the maximum number of supported cameras (from 1 to 4), the number of data lanes for each camera (from 1 to 4), and the number of data lanes at the output (again, from 1 to 4). The actual number of cameras and lanes is programmable, and can be set to any value up to the maximum values set by the compilation switches.

Features

- Output rate of up to 6Gbps
- Support all CSI2 video format with up to 16 bit per pixel[1]
- Virtual-Channel based multiplexing
- Detects and corrects ECC errors in the input packets
- Detects CRC errors in the input packets
- Programmable handling of faulty input packets
- Optional support of CSI2 DPCM compression
- Programmable timing parameters

[1] Non-legacy YUV420 data formats, with different packet lengths for Odd and Even lines, are supported only as an option

Simplified Block Diagram