SVRPlus2500

2.5Gbps Per Lane MIPI®-CSI2 Compliant Serial Video Receiver

Product Brief

September 2021

Introduction

This document is a short description of VLSI Plus Serial Video Receiver (SVRPlus2500) – a MIPI[R] CSI2, 2500Mbps per lane, serial receiver for video streams, optimized for FPGA implementations.

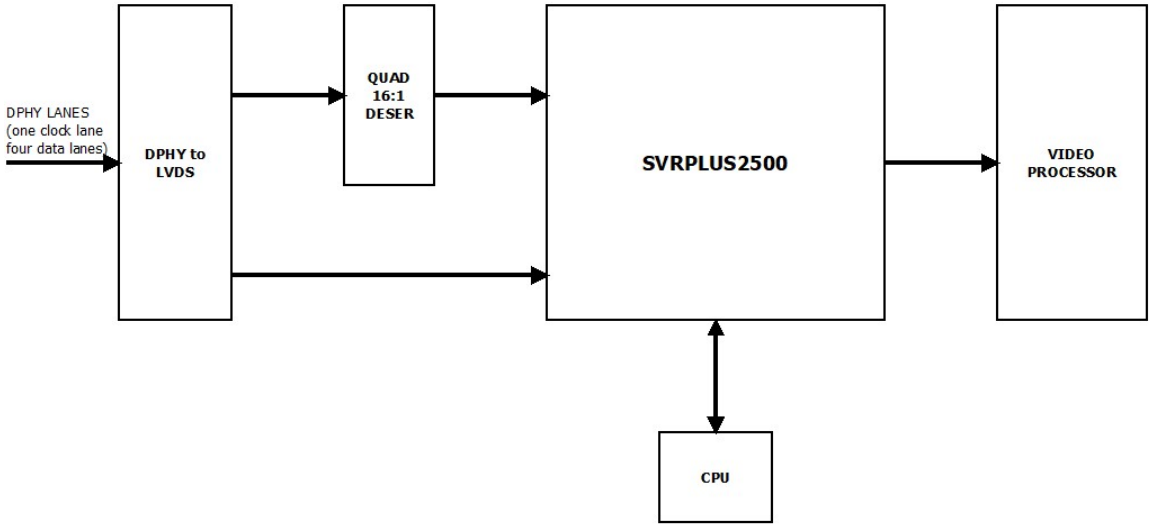
The SVRPlus supports a clock lane and up to four data lanes, each lane featuring up to 2.5Gbps, for a total of 10Gbps. The highly parallel architecture of the SVRPlus2500 allows a relatively slow internal clock of approximately 170Mhz for the most demanding configurations.

The SVRPlus2500 supports all CSI2 mandatory and optional video formats, including compressed video formats. Noise resiliency is improved using Pseudo-Random-Binary-Sequence (PRBS) encoding on the data lanes.

Compliance

The SVRPlus-CSI2-F complies MIPI CSI2 and DPHY specifications (version 2.0 of both documents).

System View



The SVRPlus2500 receives video over MIPI DPHY lanes (one clock lane and one to four data lanes), at up to 2.5Gbps per data lanes. An external DPHY to LVDS device converts the DPHY signals to LVDS signals. In the FPGA, a high-speed 16:1 DESER sends parallel low-clock-rate data to the SVRPlus2500 IP core. The SVRPlus outputs parallel video, in one to eight (and, for some video formats, one to sixteen) parallel pixels, for further processing.

A simple CPU is typically required for configuration and, if needed, for diagnostics

Features

- Configurable 1 to 4 data lanes.
- Up to 2.5Gbps per lane.
- Support of all CSI2 primary and secondary data formats.
- Optional support of Alias Datatype.
- 128-bit internal data buses, for high throughput.
- Selectable 1-, 2-, 4- or 8-pixels output per clock (1,2 or 4 for pixels with more than 16 bits).
- (With the Alias Datatype option) – support of up to 16 8-bit pixels per clock.
- Full data-compression support, including Predictor-1 and Predictor-2
- VCX (extended virtual channel) support – up to 16 channels.
- PRBS Descrambling per lane
- 16-bit deserializing (off-IP).
- Internal error registers to ease communication error diagnostics.
- Error counters for BER measurement and communication-error statistics.

Clocks

The frequency of FCLK – the main clock of the SVRPlus2500 - is relatively low, allowing easy FPGA timing closure, even when 2.5Gbps per lane is used.
FCLK frequency should be faster than the maximum of:

- Lane bitrate divided by 16.
- Pixel-rate divided by the number of parallel output pixels.

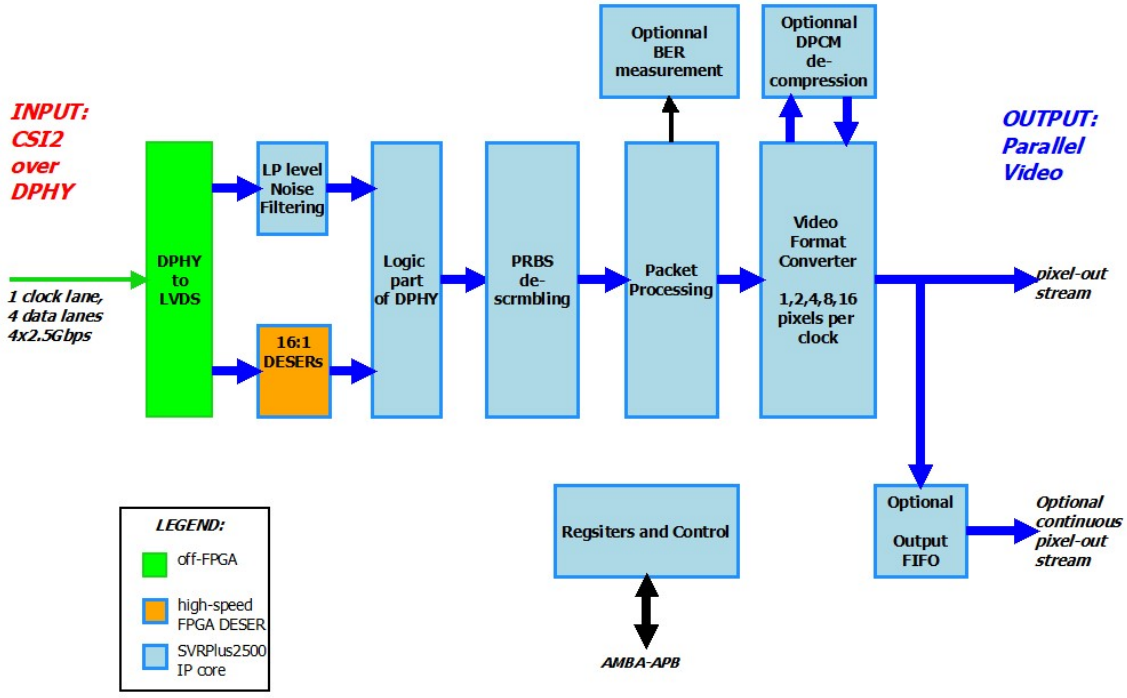
For example, a 30 FPS, 7680x4096 (8K) camera with RAW10 pixels, outputting 2.5Gbps on 4 data lanes, will require FCLK clock input with frequency greater than:

MAX(2500M/16, 960M/8) = 156.25MHz.

A second clock input (PCLK) is used for AMBA-APB register read/write, with relatively low frequency (e.g., 10MHz)

When the Output-FIFO option is ordered, a third clock – DCLK – is used to clock the pixels out of the internal FIFO. The minimum DCLK frequency is Pixel-rate divided by the number of parallel output pixels (the pixel-rate, in this case, is the average pixel rate in a video line).

Block Diagram



Flow of operation

Incoming video data over the DPHY lanes is converted by an off-FPGA device to FPGA LVDS signals, including the DPHY High-Speed and Low-Power components. FPGA-specific high speed 16:1 DESERs (one for each data lane) convert the High-Speed data to 16-bt parallel (for each data lane) format.
In the SVRPlus2500 IP core, the digital part of the DPHY specification is first executed; then, A PRBS-descrambler descrambles the input data, separately for each lane. A Packet Processor processes input packets and forwards raw data to a format converter, which decodes the data to pixels, according to the selected video format (the video format is specified in the packet header).

One, two, four or 8 (and sometimes 16), pixels, with a Pixel-Valid qualifier, are output in parallel. In addition, if the Output-FIFO option is ordered, a FIFO buffers the pixels, which can be read continuously, synchronized to a user clock (DCLK).

All configuration and monitoring registers may be accessed through an AMBA-APB interface, which also includes an Interrupt line, to inform a CPU when communication events occur.

SVRPlus-2500 Registers

NAME	FUNCTION
SVR_En_Reg	Enable SVR operation
SVR_Cfg_Reg	General Configuration
SVR_Timers_Cfg_Reg	Configuration of Timers
Int_Status_Register	Interrupt Status
Int_ Mask_Register	Interrupt Mask
Int_Read_and_Clear	Read and Clear Interrupt Status; Clear interrupt sources
BER measurement registers	Optional set of counters, for BER measurement
EPHY_Level_Indication	Debug
Current_Packet_State	Debug
Last_Packet_Indication	Debug
Protocol_Level_Indication	Debug
IP Vendor Code	Manufacturer ID assigned to VLSI Plus by MIPI[R]
Version	Unique 32 bit code for the current FPGA version