SVRPlus-CSI2-F
Extended
MIPI CSI2
High Performance
Serial Video Receiver
For FPGA Implementation

Information Brief

Introduction

This document is a short description of VLSI Plus (www.vlsiplus.com) SVRPlus-CSI2-F – a second generation high performance Serial Video Receivers for video streams, supporting MIPI® CSI2 and extensions to MIPI® CSI2, and and allowing very high performance while employing relatively low clock frequencies. The SVRPlus-CSI2-F is aimed at FPGA implementations.

The SVRPlus-CSI2-F definition and design take advantage from the long experience of VLSI Plus in providing first generation CSI2 receiver IP cores to a variety of customers. VLSI Plus SVR-CS and SVR-CS4 are used by leading CMOS image sensor vendors for the production floor testing of their sensor modules. Continued dialog with CSI2 customers in the past five years enabled us to define this new generation CSI2 receiver IP to meet current and future needs.

The SVRPlus-CSI2-F is provided with two compilation switches, which allow customer customization of the following features:

- EIGHT_LANES compilation switch – choose between MIPI® CSI2 4 lanes (switch = OFF) and extended MIPI® CSI2, with up to 8 data lanes and 2 clock lanes (switch = ON)
- PARALLEL_PIXELS switch – choose the number of output pixels per clock – by setting the switch to 1, 2 or 4.

In addition to the compilation switches, there are ordering options which measure BER rates, enhance debugging, add output FIFO, allow I2C interface and more.

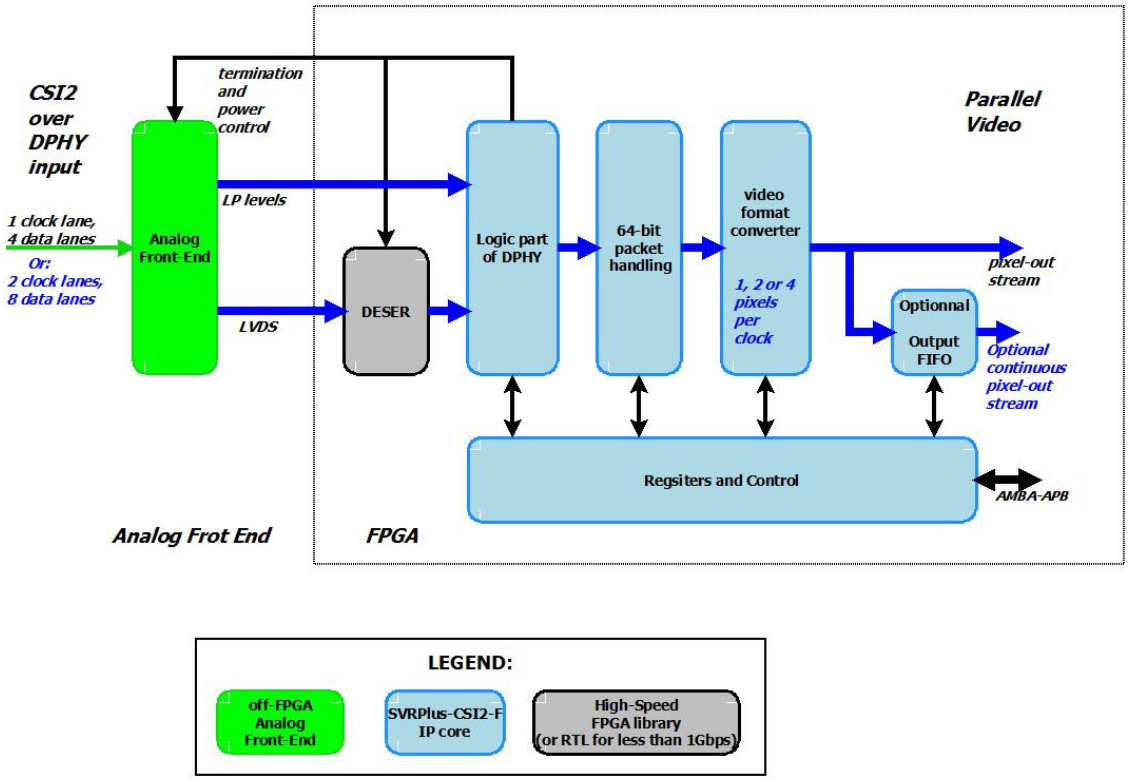
Need for Higher Data Rates

Latest and forthcoming CMOS image sensors surpass 10M pixels, and output video at 30 and even 60 fps. This development requires high bandwidth between the camera and the application processor. For example, a commercially available 4068x3456 30 fps camera outputs an average of over 5Gbps, which requires 4 DPHY lanes at more than 1.25Gbp – more the original 1Gpbs of MIPI DPHY 1.0, but still manageable by the extended 1.5Gbps of the latest DPHY spec. However, when the same or similar camera will reach 60fps, over 10Gbps will be required, and 4 lanes will not suffice.

MIPI's forthcoming new set of standards (CSI3 over UNIPRO and MPHY) will offer higher bandwidth. However, until those standards are available, camera vendors are looking for ways to increase CSI2 speed. Among others, extension of the CSI2 standard to 8 data lanes, with one or two clock lanes, are introduced.

Application processor vendors also face speed issues. Handling of 16-million-pixel frames at 60 fps requires the processing of 1G pixel per second. As employing a 1GHz clock is not desirable, the trend is to process more than one pixel in each clock cycle.

The SVRPlus-CSI2- F IP Core



VLSI Plus' SVRPlus-CSI2-F IP core is designed to support those trends, and, at the same time, work with a relatively slow clock rate, processing several pixels per clock.

The SVRPlus-CSI2-F has an internal 64-bit bus. With this bus width, 10Gbps can be handled by a reasonable167MHz clock.

The output path of the SVRPlus-CSI2-F can handle 1, 2 or 4 pixels in parallel. Image sensors which generate, for example, 12M * 60 fps = 720M pixels per second, can be handled by the SVRPlus-CSI2-F driven by a 180MHz clock, if the PARALLEL_PIXELS compilation switch is set to 4.

The SVRPlus-CSI2-F can handle up to 8 data lanes, with one or two clock lanes, and at up to 1.5Gbps per lane. If extended CSI2 is not required, the customer can save gate count and off-FPGA circuits by setting the EIGHT_LANES compilation switch to NO.

Functionality Highlights

The SVRPlus-CSI2-F IP core functionality highlights include:

- Configurable (register control) number of data lanes 1 to 4 or 1 to 8, according to the state of the EIGHT_LANES compilation switch;
- Configurable (register control) 1 or 2 clock lanes when the EIGHT_LANES compilation switch is set to ON;
- 64 bit internal data bus
- 1, 2 or 4 pixels output per clock, as set by the PARALLEL_PIXESL compilation switch
- Up to 1.5Gbps per lane;
- All CSI2 functionality implemented in hardware, freeing the CPU to other tasks
- Support of all data formats.
- Extensive set of registers, accessible by AMBA APB bus (or, optionally, by I2C)
- Programmable timing parameters
- Optional support of CSI2 compressed-video formats
- Optional output FIFO for continuous output streams
- Optional Error counting hardware, for on-line BER measurements

Clock Rates and Performance

The SVRPlus-CSI2-F main clock frequency is set by the following constraint:

$$Min(Fclk) \geq 1.05*(max(bps/8, L*bps/64, PPS/P)$$

Where:

- bps is the maximum bit rate per lane;
- L is the number of lanes in use
- pps is the pixel-per-second rate of the image
- P is the number of pixels processed in parallel (as set by the PARALLEL_PIXELS compilation switch)

Here are two examples (we assume that video is active 95% of the time; that is – horizontal and vertical blank last 5% of the overall time):

1. **10 M-pixel sensor, 4 lanes, 30 fps, RAW12; 1 pixel output per clock:**

pps = 10M * 30 / 0.95 = 316M

bps = 316M * 12 / 4 = 947M

Min(Fclk) ≥ 1.05*max(947M/8, 4*947M/64, 316M) = 331MHz

2. **12 M-pixel sensor, 8 lanes, 60 fps, RAW10; 4 pixel output per clock**

pps = 12M * 60 / 0.95 = 757M

bps = 757M * 10 / 8 = 947M

Min(Fclk) ≥ 1.05*max(947M/8, 8*947M/64, 757M/4) = 199MHz

For more information, please write to info@vlsiplus.com

Please visit our website at www.vlsiplus.com