SVTPlus2500

2.5Gbps Per Lane MIPI®-CSI2 Compliant Serial Video Transmitter

Product Brief

May 2021

Introduction

This document is a short description of VLSI Plus Serial Video Transmitter (SVTPlus2500) – a MIPI^{R} CSI2, 2500Mbps per lane, serial transmitter for video streams, optimized for FPGA implementations.

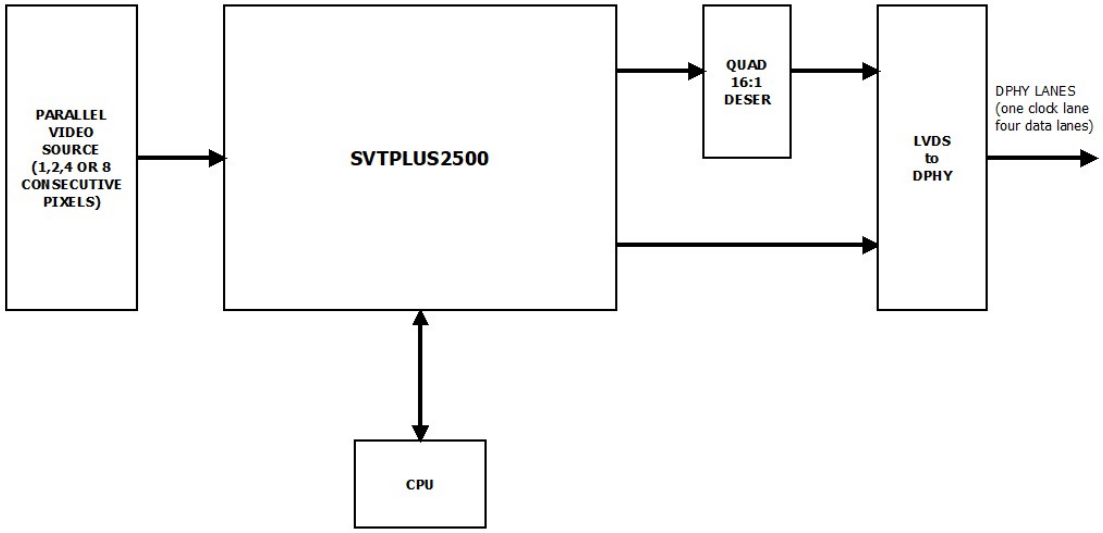
The SVTPlus supports a clock lane and 4 data lanes, each lane featuring at up to 2.5Gbps, for a total of 10Gbps. The highly parallel architecture of the SVTPlus2500 allows relatively slow internal clocks of approximately 160Mhz.

The SVTPlus supports all CSI2 mandatory and optional video formats, including compressed video formats. Noise resiliency is improved using Pseudo-Random-Binary-Sequence (PRBS) encoding on the data lanes.

Compliance

The SVTPlus-CSI2-F complies with MIPI CSI2 and DPHY specifications (version 2.0 of both documents).

System View



The SVTPlus2500 receives parallel pixels from a video source (1,2,4 or 8 pixels per clock). The pixels are translated to MIPI CSI2 packets and output from the SVTPlus2500 by high-speed parallel and low-power signals. The high-speed parallel signals are converted by an FPGA-specific high-speed 16:1 seriallizer, to DPHY high-speed signals, at up to 2.5Gbps per lane. An external LVDS to DPHY device converts the high speed and the low-power inputs to DPHY signals, transmitted over a single clock lane and up to four data lanes. A simple CPU is typically required for configuration and, if needed, for diagnostics.

Features

- Configurable 1 to 4 data lanes.
- Up to 2.5Gbps per lane.
- Support of all CSI2 primary and secondary data formats.
- 128-bit internal data buses, for high throughput.
- Selectable 1-, 2-, 4- or 8-pixel input per clock (1,2 or 4 for pixels with more than 16 bits per pixel).
- Full data-compression support, including Predictor-1 and Predictor-2.
- VCX (extended virtual channel) support – up to 16 channels.
- PRBS scrambling per lane.
- Calibration sequences for inter-lane de-skewing.
- 16-bit parallel to serial converter (off-IP).
- Configurable timing control for all DPHY parameters.
- Excel sheets for easy timing-parameter optimization.

Clocks

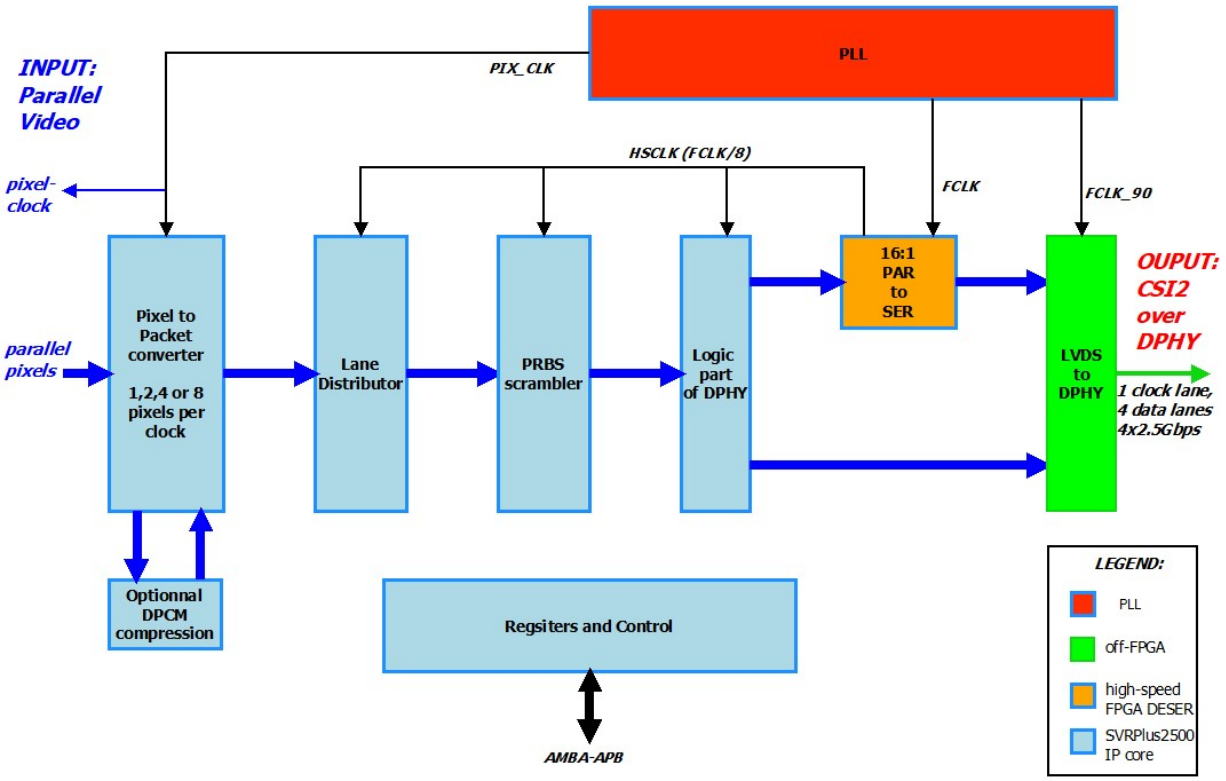
The SVTPlus2500 is driven by two main clocks – PIX-CLK and HSCLK. The frequency of the clocks is low relative to the fast bitrate and pixel-rate, allowing easy FPGA timing closure.

The PIX-CLK clock drives circuits that process incoming pixels. The frequency of PIX-CLK is equal to the pixel rate, divided by the number of input pixels per clock. For example, a 30 FPS, 7680x4096 (8K) parallel video source at 8 pixels-per-clock will require a PIX-CLK frequency of roughly 120MHz.

The HSCLK clock drives circuits that process packets. HSCLK frequency is derived from the DPHY bit rate, divided by 64. The maximum requirement, when SVTPlus2500 outputs 4 lanes each at 2.5Gbps, is 4*2.5G/64 = 166MHz.

A third clock input (PCLK) is used for AMBA-APB register read/write, with relatively low frequency (e.g., 10MHz).

Block Diagram



Flow of operation

Parallel video, at 1, 2, 4 or 8 pixels per clock, is input to the SVTPlus2500, clocked by PIX-CLK. The pixels are converted to CSI2 packets, and then distributed to four lanes. A PRBS scrambler scrambles the data, separately for each lane. Next, data is converted to DPHY digital signals, including low-power signals and parallel high-speed signals (16 bit per lane).

FPGA-specific high speed 16:1 seriallizers (one for each data lane) convert the parallel high-speed data to LVDS high-speed signals that are output from the FPGA.

An external LVDS to DPHY conversion device converts the high-speed and low-power LVDS signal to DPHY lanes.

To generate the SVTPlus2500 clocks, a PLL is required. The PLL outputs an FCLK clock (at half the lane bitrate, e.g., 1.25GHz for 2.5Gbps), an FCLK90 clock (the FCLK,

delayed by 90°), an HSCLK clock (FCLK divided by 16) and a PIX-CLK clock, with frequency equal to

FCLK-frequency * ***Lanes*** / (bit-per-pixel * ***PAR-PIXELS***)

where ***Lanes*** is the number of data lanes (up to four) and ***PAR-PIXELS*** is the number of parallel input pixels (1,2,4 or 8).

All configuration and monitoring registers may be accessed through an AMB-APB interface. For on-line configuration change, some of the configuration registers may be replaced by external inputs to the SVTPlus2500.

SVTPlus-2500 Main Registers

NAME	FUNCTION
SVT_En_Reg	Enable SVT operation
SVT_Cfg_Reg	General Configuration
SVT_Timer_Cfg_A_Reg	Configuration of Timers
SVT_Timer_Cfg_A_Reg	
SVT_Timer_Cfg_A_Reg	
SVT_EHD_LEAD	Lead time – EHD input to HD input (optional)
SVT_LAST_FRAME_COUNT	Frame-count wraparound limit
FS_VC	Virtual channel for Frame-Start
FE_VC	Virtual channel for Frame-End
LP-Header	Long packet header (without the ECC)
Secondary LP-Header	Header for secondary video formats in predefined lines
LP-EX-VC	extended virtual channel for long packets
ICR	Initial calibration sequence length
PCR	Periodic calibration sequence length
Main-BPP	bit-per-pixel for the main video lines
IP Vendor Code	manufacturer ID assigned to VLSI Plus by MIPI®
Version	Unique 32-bit code for the current FPGA version