Customizable 4/8-Lane High Throughput CSI2 Serial Video Transmitter (SVTPlus-CSI2-F)

Product Brief

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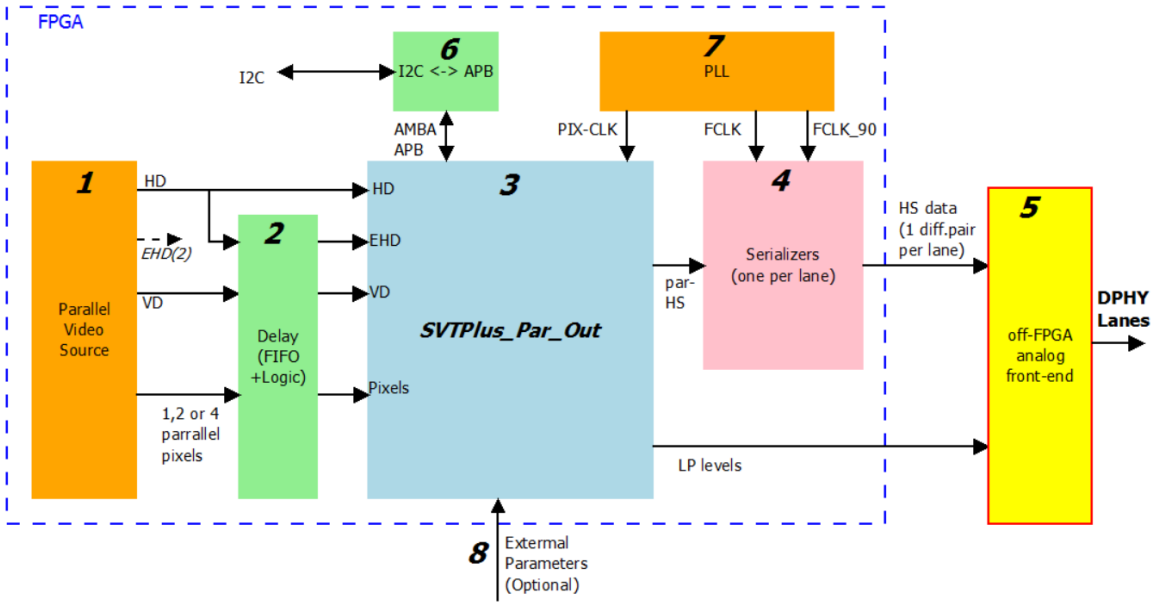
The SVTPlus-CSI2-F is a second generation MIPI CSI2-Tx transmitter IP core for FPGA implementations. It complies with MIPI® CSI2 V2.0 and DPHY1.2 specifications, with up to 8 data lanes, at up to 2.5GBPS per lane. Total available bit rate is 20Gbps, supporting, for example, 7680x4320 (8K) images at 60fps

CSI2 defines a multitude of video formats, and other optional features. The implementation of all possible optional features requires a large amount of FPGA resources and, consequently, higher power consumption. Typical applications, however, require only a small subset of the video format and other features. The SVTPlus-CSI2-F design allows customized optimization of the IP according to the required video formats and optional features. This results in optimized FPGA size and reduced power consumption.

Highlights:

- One clock lane, and from 1 to 8 data lanes (Customization-Option)
- Simple interface – legacy parallel-video input, augmented by an Early-HD signal
- Input interface – parallel 1, 2 or 4 pixels per clock (Customization-Option)
- Customized pixel-format support – can support ***any*** or ***all*** CSI2 2.0 pixel formats
- Uses simple off-FPGA analog front-end – passive or active.
- Optional DPCM compression scheme according to CSI2 specification Annex A
- Optional Calibration Packet generation.
- Easy-to-use Excel programming guide provided with the IP
- Comprehensive customer support, until IP integration is successfully completed

System Description



SVTPlus-CSI2-F System Outline

The figure above depicts the block diagram of a CSI2-over-DPHY transmitter system, built with the SVTPlus-CSI2-F IP core:

1. Input is a parallel video stream, in one of the many formats supported by MIPI CSI2. 1, 2 or 4 parallel pixels per clock are input. An HD input is active throughout the video lines, and a VD input encapsulates video frames. A typical parallel video source is any parallel-output digital camera.
2. The SVTPlus-CSI2-F requires an Early-HD (EHD) signal, to initiate the generation of long packets. Many cameras have an internal indication prior to the start of the video stream, which can be used as EHD (for example, in image sensors – start column analog to digital conversion). In those cases, Delay Unit (2) will not be needed.
   When this is not the case, an optional Delay unit is added, delaying the parallel video stream into the SVTPlus core. The original HD will be used as EHD, while pixel input, HD and VD will be delayed.
3. The SVTPlus-Par-Out is the RTL part of the IP. DPHY lanes have two modes of operation – high-speed, in which each lane is a differential transmitter, and low-power, where each of the two wires of each lane can assume different CMOS levels, as defined by the protocol. The SVTPlus-Par-Out drives the low-power levels directly, and outputs parallel bytes for the high-speed mode, which are then serialized.
4. The SVTPlus-CSI2-F delivery includes an RTL serializer, which may be used if the required high bit rates are not high. For high bit rates, the customer should use an

I/O bound high-speed serializer. Such serializers are FPGA specific, typically generated by a tool provided by the FPGA vendor. The customer is encouraged to consult with VLSI Plus on the recommended serializer for his/her specific requirements.

5. The serialized high-speed lanes, in differential LVDS pairs, along with the low-power signals generated by the SVTPlus-par-out, are output from the FPGA to an Analog-Front-End unit, which then drives the DPHY lanes. The analog front end may be DPHY compliant, in which case it is implemented by active components, or DPHY compatible, in which case passive components only are needed (but strict DPHY compliance is not provided). The customer is encouraged to consult with VLSI Plus on his/her recommended front-end solution.
6. The SVTPlus-par-out operation is governed and monitored by user accessible registers. The registers are accessed by AMBA-APB cycles. Alternatively, an I2C-to-AMBA module can be ordered, allowing I2C access to the registers.
7. Bit rate at the parallel-video input and at the DPHY lanes output must match. This is obtained by generating two clocks – FCLK for the lanes, and PIX-CLK for the input path. The frequency ratio FCLK/PIX-CLK must be equal to 2*PPC*BPP/Lanes, where PPC is the number of parallel pixels at the input (1,2 or 4), BPP is the number of bits per pixel and Lanes is the number of configured DPHY lanes. FCLK and PIX-CLK are typically generated by a PLL, along with FCLK-90 – a 90-degrees shift of FCLK, needed by the DPHY clock lane. A third clock – CPU-CLK is used for register I/O.
8. Some applications require multiplexing of several video sources, using CSI2 Virtual Channels and/or different data types. This can be done by reprogramming the video parameters in the IP registers, but for more efficient multiplexing the customer may wish to use hardware multiplexing off the IP. In this case, the IP should be ordered with the External Parameters option – the parameters will be input into the IP via additional pads, and the corresponding registers will not be implemented.

Customization and Options

Video Formats

Except for few basic video formats which are always provided, The SVTPlus-CSI2 is customized to support only the required additional video formats. This approach saves a lot of FPGA resources and eases timing closure:

Video format	Data Type	
RAW6	28	Customization Option
RAW7	29	Customization Option
RAW8	2A	STANDARD
RAW10	2B	Customization Option
RAW12	2C	Customization Option
RAW14	2D	Customization Option
RAW16	2E	STANDARD
RAW20	2F	Customization Option
RGB444	20	Customization Option
RGB555	21	Customization Option
RGB565	22	STANDARD
RGB666	23	Customization Option
RGB888	24	Customization Option
YUV420-8bit	18,1C	STANDARD
YUV420-10bit	19,1D	Customization Option
Legacy YUV420-8bit	1A	STANDARD
YUV422-8bit	1E	STANDARD
YUV422-10bit	1F	Customization Option
Generic 8-bit Long Packet	10 to 17	STANDARD

Customized Maximum number of Lanes

CSI2 rev 1.1 allows only 4 data lanes. This limitation was removed in CSI2 rev 1.2

The SVTPlus-CSI2-F supports up to 8 data lanes. The customer can custom-order the number of lanes, saving resources and pads when this number is less than 8.

Input Delay

For video sources which do not generate an EHD signal preceding the HD, an input FIFO is needed, to delay the incoming video stream and the HD and VD.

The input delay unit can be added by the customer or provided as part of the SVTPlus-CSI2 IP.

Input Delay implementation is optional

I2C to AMBA Bridge

It is possible to add an I2C to AMBA Bridge, to allow serial access to all registers.

The I2C to AMBA Bridge is optional

Registers Default Values

To simplify or even eliminate the initialization process, the customer may specify the reset values of all registers.

Customization of the registers default values is optional

DPCM Compression

When Compression option is ordered, it is possible to define any of the User-Defined Byte Based data types to indicate encoding of compressed video in accordance with Annex E of MIPI® CSI2 specifications. The compression scheme can be selected to any of the six defined types:

- 12-8-12
- 12-7-12
- 12-6-12
- 10-8-10
- 10-7-10
- 10-6-10

Using either Predictor-1 or Predictor-2.

DPCM Compression Implementation is optional

Lane Calibration (Deskew)

Lane Calibration (deskew) is not defined in DPHY1.1, and optional (mandatory for data rates beyond 1.5Gbps per lane) in DPHY1.2

Calibration implementation is optional

External Parameters

It is possible to provide some of the packet parameters from external pads. In this case the corresponding SVTPlus registers are not implemented.

External Parameters is optional